Media Release

The Future of Chips: SMART Announces Successful Way to Commercially Manufacture Novel Integrated Silicon III-V Chips

MIT's Research Enterprise in Singapore has developed a commercially viable way to create new Silicon III-V Chips, paving the way for intelligent optoelectronic and 5G devices

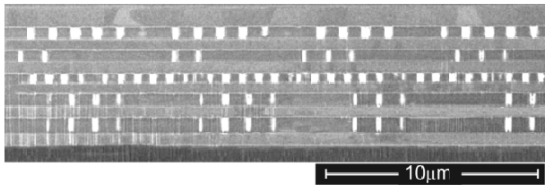
- Commercially viable manufacturing process will make integrated Silicon III-V Chips available by 2020
- New Singapore-developed method does not require tens of billions in industry investments - leveraging old 200 mm manufacturing technology and breathing new life into mature and depreciated manufacturing infrastructure
- Integrated Silicon III-V chips will enable intelligent illumination and displays, and also overcome potential problems with 5G mobile technology.

LEES researcher reviewing a 200 mm Silicon III-V wafer. The innovative and commercial-ready process by LEES leverages existing 200 mm semiconductor manufacturing infrastructure to create a new generation of chips that combines traditional Silicon with III-V devices, something not commercially viable before.

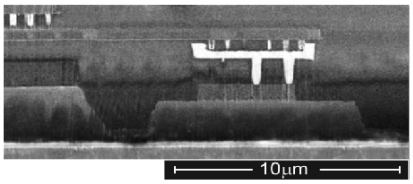
Singapore, 30 September 2019: The Singapore-MIT Alliance for Research and Technology (SMART), MIT's Research Enterprise in Singapore, has announced the successful development of a commercially viable way to manufacture integrated Silicon III-V Chips with high-performance III-V devices inserted into their design.

In most devices today, silicon-based CMOS chips are used for computing, but they are not efficient for illumination and communications, resulting in low efficiency and heat generation. This is why current 5G mobile devices on the market get very hot upon use and would shut down after a short time.

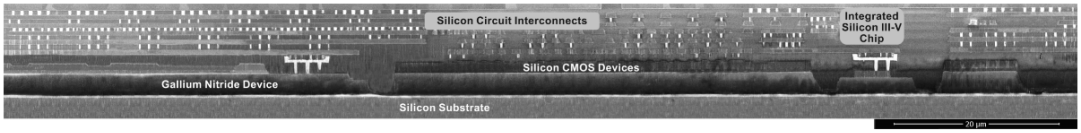
This is where III-V semiconductors are valuable. III-V chips are made from elements in the 3rd and 5th columns of the elemental periodic table such as Gallium Nitride (GaN) and Indium Gallium Arsenide (InGaAs). Due to their unique properties, they are exceptionally well suited for optoelectronics (LEDs) and communications (5G etc) - boosting efficiency substantially.



Inset A: Zoomed in view of standard Silicon circuit interconnects.



Inset B: Zoomed in view of III-V device



Cross section of SMART's Integrated Silicon III-V chip.

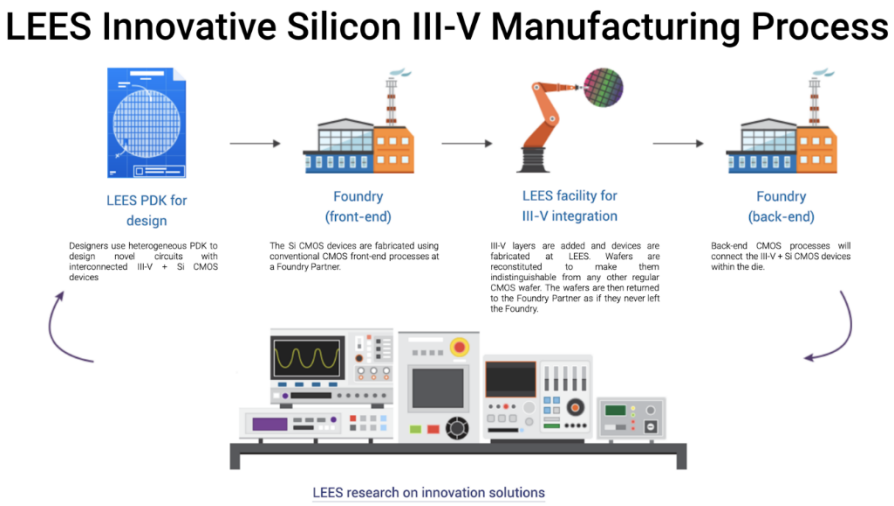
"By integrating III-V into silicon, we can build upon existing manufacturing capabilities and low-cost volume production techniques of silicon and include the unique optical and electronic functionality of III-V technology," said Eugene Fitzgerald, CEO and Director, SMART, MIT's Research Enterprise in Singapore. "The new chips will be at the heart of future product innovation and power the next generation of communications devices, wearables and displays."

Kenneth Lee, Senior Scientific Director of the SMART LEES research program adds: "However, integrating III-V semiconductor devices with silicon in a commercially viable way is one of the most difficult challenges faced by the semiconductor industry, even though such integrated circuits have been desired for decades. Current methods are expensive and inefficient, which is delaying the availability of the chips the industry needs. With our new process, we can leverage existing capabilities to manufacture these new integrated Silicon III-V chips cost-effectively and accelerate the development and adoption of new technologies that will power economies."

The new technology developed by SMART builds two layers of silicon and III-V devices on separate substrates and integrates them vertically together within a micron, which is 1/50th the diameter of a human hair. The process can use existing 200mm manufacturing tools, which will allow semiconductor manufacturers in Singapore and around the world to make new use of their current equipment. Today, the cost of investing in a new manufacturing technology is in the range of tens of billions of dollars, thus this new integrated circuit platform is highly cost-effective and will result in much lower cost novel circuits and electronic systems.

SMART is focusing on creating new chips for pixelated illumination/display and 5G markets, which has a combined potential market of over $100B USD. Other markets that SMART's new integrated

Silicon III-V chips will disrupt include wearable mini-displays, virtual reality applications, and other imaging technologies.



The patent portfolio has been exclusively licensed by New Silicon Corporation Pte. Ltd. (NSC), a Singapore-based spin-off from SMART. NSC is the first fabless silicon integrated circuit company with proprietary materials, processes, devices, and design for monolithic integrated Silicon III-V circuits (www.new-silicon.com).

SMART's new integrated Silicon III-V chips will be available next year and expected in products by 2021.

High resolution images are available at this link.

###

About Low Energy Electronic Systems (LEES) Interdisciplinary Research Group (IRG)

SMART's Low Energy Electronic Systems (LEES) IRG is creating new integrated circuit technologies that result in increased functionality, lower power consumption and higher performance for electronic systems. These integrated circuits of the future will impact applications in wireless communications, power electronics, LED lighting, and displays. LEES has a vertically-integrated research team possessing expertise in materials, devices, and circuits, comprising multiple individuals with professional experience within the semiconductor industry. This ensures that the research is targeted to meet the needs of the semiconductor industry both within Singapore and globally.

For more information, please logon to: http://www.circuit-innovation.org

About Singapore-MIT Alliance for Research and Technology (SMART)

Singapore-MIT Alliance for Research and Technology (SMART) is MIT's Research Enterprise in Singapore, established by the Massachusetts Institute of Technology (MIT) in partnership with the National Research Foundation of Singapore (NRF) since 2007. SMART is the first entity in the Campus for Research Excellence and Technological Enterprise (CREATE) developed by NRF. SMART serves as

an intellectual and innovation hub for research interactions between MIT and Singapore. Cutting-edge research projects in areas of interest to both Singapore and MIT are undertaken at SMART. SMART currently comprises an Innovation Centre and six Interdisciplinary Research Groups (IRGs): Antimicrobial Resistance (AMR), BioSystems and Micromechanics (BioSyM), Critical Analytics for Manufacturing Personalized-Medicine (CAMP), Disruptive & Sustainable Technologies for Agricultural Precision (DiSTAP), Future Urban Mobility (FM) and Low Energy Electronic Systems (LEES).

SMART research is funded by the National Research Foundation Singapore under the CREATE programme. For more information, please visit - http://smart.mit.edu

For media queries, please contact:
Tazkira Sattar
SMART@bluetotem.co
+65 8280 3055